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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

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Sheet 1 of 6

**Complete if Known**

Application Number	10/005,105
Filing Date	December 3, 2001
First Named Inventor	Paul C. Kocher
Art Unit	2132
Examiner Name	Abdulhakim Nobahar
Attorney Docket Number	44424162-8721

**U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (If known)			
/H.N./	V70	US 2,632,058 B1	03-17-1953	Gray	
	V71	US 2,733,432 B1	01-31-1956	Breckman	
	V72	US 3,816,762 B1	06-11-1974	Holt Jr.	
	V73	US 4,268,898 B1	05-19-1981	Brown	
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	V75	US 4,570,084 B1	02-11-1986	Griffin et al.	
	V76	US 4,622,480 B1	11-11-1986	Uchimura et al.	
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	V80	US 4,937,649 B1	06-26-1990	Shiba et al.	
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	V83	US 5,399,996 B1	03-21-1995	Yates et al.	
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/H.N./	V94	US 5,821,775 B1	10-13-1998	Mehta et al.	

Examiner  
Signature

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Date  
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07/17/2008

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/H.N./	V95	US 5,859,548 B1	01-12-1999	Kong	
↓	V96	US 5,905,399 B1	05-18-1999	Bosnyak et al.	
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	V103	US 6,107,835 B1	08-22-2000	Blomgren et al.	
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/H.N./	V106	US 6,442,525 B1	08-27-2002	Silverbrook et al.	

**FOREIGN PATENT DOCUMENTS**

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		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				
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/Abdulahkim Nobahar/

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				First Named Inventor	Paul C. Kocher
				Group Art Unit	2132
				Examiner Name	Abdulahakim Nobahar
Sheet	3	of	6	Attorney Docket No.	44424162-8721
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/H.N./	V107	DAVIES & PRICE, Security for Computer Networks: An Introduction to Data Security in Teleprocessing and Electronic Funds Transfer, John Wiley & Sons, New York, NY, 2nd Ed., 1989, 377 pages (entire book).			
	V108	Defendant VISA International Service Association's Final Invalidity Contentions for U.S. Patent No. 6,304,658 Pursuant to Patent L.R. 3-6(b), February 8, 2008, Case No. C04-04143 JW(HRL), U.S. District Court, Northern District of California, San Jose Division.			
	V109	Defendant VISA International Service Association's Final Invalidity Contentions for U.S. Patent No. 6,381,699 Pursuant to Patent L.R. 3-6(b), February 8, 2008, Case No. C04-04143 JW(HRL), U.S. District Court, Northern District of California, San Jose Division.			
	V110	Defendant VISA International Service Association's Final Invalidity Contentions for U.S. Patent No. 6,510,518 Pursuant to Patent L.R. 3-6(b), February 8, 2008, Case No. C04-04143 JW(HRL), U.S. District Court, Northern District of California, San Jose Division.			
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/H.N./	V114	DRAPER, Don et al., "Circuit Techniques in a 266-MHz MMX-Enabled Processor", <i>IEEE J. Solid State-Circuits</i> , pp. 1650-1664, November 1997.			
Examiner Signature	/Abdulahakim Nobahar/			Date Considered	07/17/2008

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		Application Number	10/005,105		
		Filing Date	December 3, 2001		
		First Named Inventor	Paul C. Kocher		
		Group Art Unit	2132		
		Examiner Name	Abdulahakim Nobahar		
Sheet	4	of	6	Attorney Docket No.	44424162-8721
<b>OTHER ITEMS – NON PATENT LITERATURE DOCUMENTS</b>					
Examiner Initials*	CiteNo. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T <sup>2</sup>
/H.N./	V115	EBERLE, Hans & THACKER, Charles P., "A 1 GBIT/Second GAAS DES Chip", <u>Proceedings of the 1992 IEEE Custom Integrated Circuits Conference</u> , May 3-6, 1992.			
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/H.N./	V123	KARLSSON, Magnus et al., "Implementation of bit-serial adders using robust differential logic," <u>Proc. IEEE Nordic Event in ASIC Design Conf.</u> , NORCHIP'97, Tallin, Estonia, Nov 10-11, 1997.			
	V124	LARSSON, Patrik, " <u>di/dt Noise in CMOS Integrated Circuits</u> ", <u>Analog Integrated Circuits and Signal Processing</u> , 14:113-129, Kluwer Academic Publishers, Boston, MA, 1997.			
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	V126	LOY, James R., "Managing Differential Signal Displacement", thesis, Rensselaer Polytechnic Institute, Troy, New York, August 1993.			
	V127	MAIER, Cliff A. et al., "A 533-MHz BiCMOS Superscalar RISC Microprocessor", <u>IEEE Journal of Solid-State Circuits</u> , 32(11):1625-1634, November 1997.			
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	V130	MALEKI, M. & KIAEI, S., "Enhancement Source-Coupled Logic for Mixed-Mode VLSI Circuits", <u>IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing</u> , 39(6):399-402, June 1992.			
/H.N./	V131	OKLOBDZIJA, Vojin G., "Differential and Pass-Transistor CMOS Logic for High-Performance Systems", <u>Proc. 21<sup>st</sup> International Conference on Microelectronics (MIEL'97)</u> , 2:803-810, Nis, Yugoslavia, September 14-17, 1997.			
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	V134	TABOR, Jeff F., "Noise Reduction Using Low Weight and Constant Weight Coding Techniques", dissertation, Massachusetts Institute of Technology, May 11, 1990, Cambridge Massachusetts.			
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	V136	TALLINI, Luca G. & BOSE, Bella, "Design of Balanced and Constant Weight Codes for VLSI Systems", <u>IEEE Transactions on Computers</u> , 47(5):556-572, May 1998.			
	V137	TEXAS INSTRUMENTS, SN54LS138, SN54S138, SN74LS138, SN74S138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS, Texas Instruments, Dallas, Texas, revised March 1988.			
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/H.N./	V139	WILLIAMS, Ted E. & HOROWITZ, Mark, "Bipolar Circuit Elements Providing Self-Completion-Indication", <u>IEEE Journal of Solid-State Circuits</u> , 25(1):309-312, February 1990.			
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